REMARKS

Applicant graciously acknowledges the statement that claims 7-9 and 13-14 are allowed. No claims have been amended. No new matter has been included. Claims 1-14 are now pending in this application.

Claims 1-6 and 10-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's admitted prior art ("AAPA") in combination with Tsukamoto (U.S. Patent No. 5,047,818). The rejection is respectfully traversed.

The present invention relates to a pixel cell with a gate controlled charge storage region. The present invention provides a gate controlled buried channel to obtain efficient charge transfer from the photodiode through a transistor gate as a shutter to the charge storage region where charge is stored until the charge is transferred to a sensing node, all with low charge loss. The control gate of the present invention controls the charge storage region and helps to transfer charge to the charge storage region in conjunction with the first transistor. Independent claims 1 and 11 each recite a pixel cell comprising, *inter alia*, "a photo-conversion device that generates charge," "a gate controlled charge storage region that stores the charge under control of a control gate," and "a first transistor."

Applicant respectfully submits that AAPA in combination with Tsukamoto fails to teach or suggest "a gate controlled charge storage region that stores the charge under control of a control gate," as recited by claims 1 and 11. AAPA simply refers to a typical pixel cell having an electronic shutter, which includes a shutter transistor and a storage device and does not refer to a separate control gate for controlling a charge storage region and helping to transfer charge to the charge storage region in conjunction with a first transistor. Applicant respectfully submits that the shutter transistor of AAPA, if anything, is equivalent to or similar to the "first transistor"

recited in the claimed invention and does not also relate to the recited "control gate." In other words, AAPA does not teach or suggest the use of a separate and distinct "control gate" in conjunction with the storage region.

The charged storage region because of this additional control gate is capable of maintaining the charge below the surface of the substrate minimizing recombination and charge loss. As a result, the "control gate" of the claimed invention increases the charge transfer efficiency for the pixel cell over a typical pixel cell such as the one described in the AAPA. Thus, AAPA does not, and cannot teach or suggest "a control gate," because it simply does not refer to such an element, much less, "a gate controlled charge storage region that stores the charge under control of [the] control gate." Consequently, AAPA does not teach or suggest all limitations of independent claims 1 and 11.

The Office Action attempts to cure the deficiencies of AAPA by combining it with Tsukamoto. The Office Action specifically asserts that it would have been obvious to one of ordinary skill in the art to incorporate Tsukamoto's memory cell charge storage region in the AAPA pixel circuit and maintains its previous position that one of ordinary skill in the art would have been motivated to combine AAPA and Tsukamoto to "prevent soft errors caused in the charge storage capacitor." (Office Action at 2). Applicant respectfully disagrees.

As articulated in Applicant's previous Response, Tsukamoto's teachings do not relate to pixel cells, but generally relate to a memory device and addresses the totally different problem of soft errors, and are therefore not relevant. Specifically, Tsukamoto teaches that the structure of the P-type layer 101 reduces soft errors in the capacitor, which translates into the erroneous storage of a "1" or "0" digital logic state. Tsukamoto at column 3, lines 40-44. Tsukamoto is designed to store voltages

representing 1s and 0s whereas the claimed invention, in contrast, is designed to reduce charge recombination and improve the charge transfer of electrons corresponding to an image.

One of ordinary skill in the art at the time of invention would not have looked to the memory device of the cited reference to achieve the improved "pixel cell" of the claimed invention in which charge loss at the storage region is reduced due to the presence of the control gate. Soft errors is not a problem in imagers. Indeed, imagers do not have soft errors. Instead, imagers store low charge levels representing incident light. Recombination of charge carriers, and efficient transfer of charge carriers are problems in imagers which <u>are not</u> addressed in any way by Tsukamoto. Thus, Tsukamoto would not have taught one of ordinary skill in the art to transfer a charge within a pixel cell from a photodiode to a charge storage region through a transistor and storing the charge in a charge storage region of a pixel by a control gate.

Applicant respectfully submits that Tsukamoto simply does not teach how one skilled in the art could modify the AAPA to provide a pixel cell with an electrical shutter having improved charge transfer efficiency and minimal charge loss. As a result, there is no motivation evidenced in the references to suggest combining these teachings to achieve the claimed invention. Those of ordinary skill in the art would not have been so motivated. In essence, the Examiner has used the present specification as a roadmap attempting to construct the claimed invention from the cited references based on hindsight.

Accordingly, AAPA in combination with Tsukamoto fails to teach or suggest "a gate controlled charge storage region that stores the charge under control of a control gate," and thus cannot establish a *prima facie* case of obviousness as to independent claims 1 and 11. Claims 2-6 and 10 depend from claim 1 and should be

allowable along with claim 1. Claim 12 depends from claim 11 and should be allowable along with claim 11. For at least the reasons set forth above as well as others, Applicant respectfully requests that the rejection as to all claims be withdrawn.

In view of the above amendment, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

By _____

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